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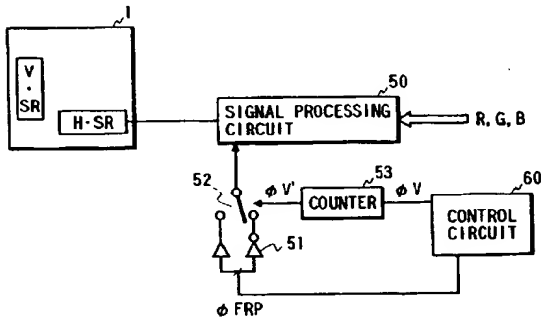
## (54) DC compensation for interlaced display

(57) In a display where an image signal is inputted to the same row of a display section at an odd field period and an even field period, even if an AC driving is performed, a problem of a deterioration of a device due to a burning of a liquid crystal of an image display section by inputting the image signal including a still image such as a character or the like. Therefore, the polarity of the image signal is inverted every field and the polarity is further inverted every arbitrary n frames. In the n-frame inversion, a 1-field inversion pulse, for example, ϕFRP that is outputted from a control circuit, is further converted to an arbitrary n-frame inversion pulse by using an inverter, a switch, a counter, and the like. Thus, a signal processing circuit converts the image signals (R, G, B) to image signals whose polarities are inverted every one field and n fields.

FIG. 1A

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## BACKGROUND OF THE INVENTION

### Field of the Invention

The present invention relates to a display and its driving method and, more particularly, to a display for inputting an image signal of an AC voltage to each pixel and its driving method.

### Related Background Art

In recent years, a multimedia is highlighted more and more or the like and an amount of information that is handled in the society is rapidly increasing. In such a situation, in place of a CRT (Cathode Ray Tube), a thin type flat display as an interface from a computer to a human being becomes an important device to widen a multimedia market. As flat displays, an LCD (liquid crystal display), a PDP (plasma display), and an electron beam flat display are leading devices. Among them, the liquid crystal display is widening a big market in association with a widespread of small type personal computers. In the liquid crystal displays, an active matrix liquid crystal display has no crosstalk as compared with a simple matrix liquid crystal display of an STN (super twisted nematic) type or the like, so that the active matrix LCD has a large contrast as a whole picture plane. Such an active matrix LCD is, therefore, attracted as not only a display of the small type personal computer but also a view finder of a video camera, a projector, and a thin type television.

As an active matrix liquid crystal display, there are a TFT (thin film transistor) type display and a diode type display. Fig. 10A is a block diagram of an image signal input of a TFT type image display. Reference numeral 10 denotes an image pixel section having pixels arranged in a matrix shape; 20 a vertical scanning circuit for selecting a display row; 30 a sampling circuit of a color image signal; and 40 a horizontal scanning circuit for generating a signal of the sampling circuit.

A unit pixel of the display pixel section 10 comprises a switching element 11, a liquid crystal material 15, and a pixel capacitor 12. In the case where the switching element 11 is a TFT (thin film transistor), a gate line 13 connects a gate electrode of the TFT and the vertical scanning circuit 20. A common electrode 21 of an opposite substrate commonly connects terminals of one side of the pixel capacitor 12 of all of the pixels. A common electrode voltage $V_{LC}$ is applied to the common electrode 21. When the switching element 11 is a diode (including a metal/insulator/metal element), a scan electrode is arranged in the lateral direction on the opposite substrate and is connected to the vertical scanning circuit 20. An input terminal of the switching element 11 is connected to the sampling circuit 30 by a data line 14 in the vertical direction. In the case where the switching element 11 is any one of the TFT and the diode, the vertical direction data line 14 connects the input terminal of the switching element 11 and the sampling circuit 30. An output terminal of the switching element 11 is connected to another terminal of the pixel capacitor 12.

A control circuit 60 separates an image signal to signals necessary to the vertical scanning circuit 20, horizontal scanning circuit 40, a signal processing circuit 50, and the like. The signal processing circuit 50 executes a gamma process considering liquid crystal characteristics, an inverting signal process to realize a long life of the liquid crystal, and the like and generates color image signals (red, blue, and green) to the sampling circuit 30.

Fig. 10B is a detailed equivalent circuit diagram of the color display pixel section 10 of the TFT type and the sampling circuit 30. The pixels (R, G, B) are arranged in a delta shape and the pixels of the same color are distributed to both sides of the data lines 14 (d1, d2, ...) every row and are connected to the data lines (d1, d2, ...). The sampling circuit 30 is constructed by switching transistors (sw1, sw2, ...) and a capacitor (a parasitic capacitance of the data lines 14 and a pixel capacitance). An image signal input line 16 is constructed by signal lines only for R, G, B colors. The switching transistors (sw1, sw2, ...) sample the color signals of the image signal input line 16 in accordance with pulses (h1, h2, ...) from the horizontal scanning circuit 40 and transfer the color signals to the pixels through the data lines 14 (d1, d2, ...). Pulses ($\phi$g1, $\phi$g2, ...) are transmitted from the vertical scanning circuit 20 to TFT gates of the pixels and rows are selected, thereby writing the signals to the pixels. As mentioned above, the pulses ($\phi$g1, $\phi$g2, ...) turn on the TFTs 11 included in the rows, so that an image signal of one horizontal scan of each corresponding row is written to all of the pixels included in the rows. The image signal of one horizontal scan is called a 1H signal hereinbelow.

Fig. 11A shows an example of an interlace scan of a liquid crystal display having rows of the same number as that of the vertical scanning lines of an image signal for a CRT type television based on the NTSC or the like. In the liquid crystal display, when the 1H signal is written to two rows, since a flickering of a motion image decreases, a 2-row simultaneous driving or a 2-row interpolation driving (signal writing corresponding to the pixels arranged in a delta shape) which is treated similarly to the 2-row simultaneous driving is often executed. In those driving methods, a combination of two rows to be selected is changed in accordance with the odd field and the even field. In the following description, it is assumed that the rows on the display pixel section which are selected and to which information is written are designated by symbols (g1, g2, ...) of vertical scanning pulses. In the odd field, the 1H signal of a horizontal scan line oddl is

written to the rows g2 and g3. Similarly, the 1H signal of odd2 is written to the rows g4 and g5. Each of the 1H signals of odd3 and subsequent horizontal scan lines is also similarly written for every two rows. On the other hand, in the even field, a combination of rows to be selected is deviated from the odd field by one row and the 1H signal of a horizontal scan line even1 is written to the rows g1 and g2. Similarly, the 1H signal of even2 is written to the rows g3 and g4 and each of the subsequent signals is also similarly written for every two rows.

Fig. 12 shows a timing chart of scan pulses of the 2-row simultaneous driving. In the odd field, the vertical scan pulses $\phi g2$ and $\phi g3$ are set to the "H" level. The TFT corresponding to each of the pixels of the rows is turned on, thereby writing the 1H signal of odd1 to the rows g2 and g3. In this instance, for the "H" period of the horizontal scan pulses (h1, h2, ...), the image signal sampled by the sampling circuit is written to the pixels of the rows g2 and g3. A similar writing operation is also executed in the scan of odd2 and subsequent lines.

Fig. 11B shows an example of the interlace scan of a liquid crystal display having rows of the number that is 1/2 of the number of vertical scan lines of the image signal for the CRT type television based on the NTSC or the like. In this case, the rows to be selected on the display pixel section are also shown by the symbols (g1, g3, ...) of the horizontal scan pulses. In the odd and even fields, the 1H signal is written to the same row. In the odd field, the 1H signal of the horizontal scan line odd1 is written to the row g2 and the 1H signal of odd2 is written to the row g4. Similarly, each of the 1H signals of odd3 and subsequent lines is also written. In the even field as well, the 1H signal of even1 is written to the row g2 and the 1H signal of even2 is written to the row g4. Each of the subsequent signals is also similarly written by using rows (g4, g8, ...) to which the information was written in the odd field. A timing chart of the scan pulse shows a scan by the 2-row simultaneous driving shown in Fig. 12 without the odd row pulses ($\phi g3$, $\phi g5$,...).

In the liquid crystal display, when a predetermined voltage is applied to a liquid crystal material for a long time, a burning phenomenon such that quality of the liquid crystal material is worse. Therefore, the image signal is written from the reference potential by the positive or negative polarity, thereby executing an AC driving in which the polarities of the image signal are exchanged. When an exchanging period of the signal polarities is long, a flickering such that a flickering is visibly recognized by the eyes of the human being appears. Fig. 13A shows signal polarities of the selected rows in the 2-row simultaneous driving. A case where the voltage of the image signal is positive for the common electrode voltage as a reference potential is expressed by "+" and a case where it is negative is expressed by "-". Each field scan period is shown in the lateral direction. A selected row is shown in the vertical direction. The signal polarities are exchanged every horizontal scan. In this case, when an attention is paid to one selected row (for example, row g2), the signal polarities are inverted every two fields. Therefore, a line flicker of 30 Hz of 1/2 of the scan period (60 Hz) of one field occurs and becomes a flickering of the display. As a frequency of the flicker is low, the flicker is recognized to the human eyes and becomes conspicuous. Particularly, when the flicker period decreases to 50 Hz or less, it is seen as a flicker to the human eyes. Therefore, there is an example such that the signal polarity of each row is inverted every field and the flicker period is set to 60 Hz. Fig. 13B shows the 2-row simultaneous driving in which the signals of the same polarity are written in the odd fields and the signals of different polarities are written in the even fields and the signal polarities are exchanged every field when an attention is paid to any row. In this case, the flicker period is set to 60 Hz and is hard to be recognized to the human eyes.

In the AC driving, the flicker is made inconspicuous by reducing the writing period of the signal to the pixel. However, there is a case where even if the writing period is set to the shortest period, when still information such as a character or the like is displayed for a long time, a burning of the liquid crystal material occurs. For example, the case where the whole picture plane is displayed in black by the 2-row simultaneous driving and only a certain portion is displayed in white will now be considered. First, an attention is paid to an example of the scan when an NTSC signal is displayed at a high fidelity to a CRT television or a display that is almost equivalent thereto. Fig. 14 shows an example of such a scan. In Fig. 14, scan lines even2, odd2, and even3 denote 1H signals of the white display and the other scan lines indicate black display signals (the signals of the black display are omitted). Since those displays display the original image signal as it is at a high fidelity, by performing the AC driving, even if a still image is displayed, there is no fear of occurrence of the burning of the liquid crystal material.

Fig. 15A shows an example of a scan when the same NTSC signal is displayed by the 2-row simultaneous driving. In the odd field, the 1H signal (original signal o2, pseudo signal o'2) of odd2 is written to the rows g4 and g5. In the even field, the 1H signal (original signal e2, pseudo signal e'2) of even2 is written to the rows g3 and g4. The 1H signal (original signal e3, pseudo signal e'3) of even3 is written to the rows g5 and g6. In this instance, the signal which is inverted every field is written to each row. Fig. 15B shows a signal voltage waveform of each row. The upper side than the reference potential ($V_{LC}$) shows an odd field period of Fig. 15A. The lower side shows an even field period. The rows in which the white display signal was written in the odd field period are only the rows

g4 and g5. The rows in which the white display signal was written in the even field period are the four rows g3, g4, g5, and g6. In this instance, the rows g3 and g6 are displayed in black in the odd field and are displayed in white in the even field. Namely, the voltages of the hatched portions remain as Dc voltages in the liquid crystal. When such a state is left for a long time, even if the AC driving is executed, there is a fear of occurrence of the burning of the liquid crystal material.

Fig. 16A shows an example of a scan when the NTSC signal is displayed by a liquid crystal display in which the number of rows is only 1/2 of the number of scan lines of the signal as described in Fig. 5. The 1H signal of odd1 and the 1H signal of even1 are written to the same row g2 and the signals of odd2 and even2 are written to the same row g4. The signals are subsequently written in a manner similar to the above. even2, odd2, and even3 show white display signals and the other scan lines show black display signals. Fig. 16B shows a signal voltage waveform of each row. In this case as well, in the row g6, the voltage of the hatched portion remains as a DC voltage in the liquid crystal and if such a state is left for a long time, there is a fear of occurrence of the burning of the liquid crystal material. Even in the plasma display, electron beam flat display, and electroluminescence display, there is a case where the devices are deteriorated such that the electrodes are corroded or the like in the DC driving, so that there is a case where the AC driving is performed. Consequently, in a manner similar to the liquid crystal display as described above, when a still image is inputted, even if the AC driving is executed, the DC voltage remains and there is a fear of deterioration of the device.

To solve the above problems, there is a liquid crystal display such that a television signal which handles a motion image is 2-line simultaneous interlace driven and a still image such as character information or the like is 2-line simultaneous non-interlace driven (Japanese Patent Application No. 3-94589). However, in such a liquid crystal display, if there is a still image portion in the television signal, a burning occurs. To prevent it, it is necessary to use a frame memory, a motion detecting circuit, or the like to judge whether the image is a motion image or a still image, so that the apparatus becomes very complicated and expensive.

## SUMMARY OF THE INVENTION

In consideration of the above problems, it is a subject of the invention to provide a display which doesn't cause a burning even when a still image signal such as a character or the like is inputted by adding a simple circuit.

The present inventors had made efforts to solve the above subject, so that the following invention was obtained. That is, according to the invention, there is provided a display having a case where an image signal is inputted to the same row in an odd field period and an even field period, wherein the display has means for inverting a polarity of the image signal every field and, further, for inverting the polarity every arbitrary frames. The invention also incorporates the invention of a driving method of the display. That is, according to the invention, there is provided a driving method of a display having a case where an image signal is inputted to the same row in an odd field period and an even field period, wherein a polarity of the image signal is inverted every field and, further, the polarity is inverted every arbitrary frames.

The n-frame inversion can be realized by further converting the 1-field inverting pulse of 1H such as $\phi$FRP to an arbitrary n-frame inverting pulse by using an inverter 51, a switch 52, a counter 53, and the like as shown in Fig. 1A. Fig. 1B shows a timing chart of the polarity of an image signal that is inputted to a certain element in the display of the invention when paying an attention to such an element. While the polarity of the image signal that is inputted to the element is inverted every field, the polarity is also inverted for a period of a further large n-frame. The value of (n) is preferably set to an integer. However, it is also possible to set the value of (n) to a small number so long as the polarity inversion of a large period occurs in a writing period of one field. It is desirable that an arbitrary n-frame inversion is performed in a range where it is not perceived by the human eyes. Since the ordinary liquid crystal is burned for a time interval from a few minutes to a few hours, it is sufficient to invert the polarity within such a range. For example, it is desirable to execute such an arbitrary frame inversion at a period of time from 0.13 second (7.5 Hz) to 60 minutes, more preferably, from one second (1 Hz) to one minute.

Figs. 2A to 2D show field inverting systems to which the invention can be applied. In the diagram, Fig. 2A shows a 1-field inverting system, Fig. 2B a 1H/1-field inverting system, Fig. 2C a data line/1-field inverting system, and Fig. 2D a bit/1-field inverting system. In the invention, in addition to those inverting systems, the polarity is further inverted at arbitrary n frames.

The invention can be also applied to any displays such that even if the AC driving is performed, the DC component remains in the image signal inputted to the pixel. For example, as such displays, there are a liquid crystal display, a plasma display, an electron beam flat display, an electroluminescence display, and the like.

In the invention, since the DC components such as rows g3 and g6 in Fig. 15B or the row g6 in Fig. 16B are exchanged every n frames, the liquid crystal is not burned. In case of using the liquid crystal display as a display of the invention, since a still image signal which became the DC component hitherto is inverted

at a period larger than the field, the liquid crystal material is not burned. When the display of the invention is either one of the plasma display, electron beam flat display, and electroluminescence display, since the still image signal which became the DC component hitherto is inverted at a period larger than the field, the element is not deteriorated. Therefore, a display with a high reliability can be provided for a long time.

## BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A and 1B show block diagrams Fig. 1A of a circuit to execute an n-frame inversion of the invention and an image signal Fig. 1B constructed by n frames;
Figs. 2A to 2D show examples of inverting systems;
Fig. 3 is a block diagram of a circuit in which image signal input units of two systems are provided for a liquid crystal display;
Fig. 4 is a detailed diagram of a display pixel unit, a storage circuit, and a sampling circuit;
Fig. 5 is a timing chart for an image signal input;
Fig. 6 is a block diagram of a circuit to execute an n-frame inversion;
Fig. 7 shows an example of a buffer circuit;
Fig. 8 shows an example in which different kinds of pixels are connected to the same data line;
Fig. 9 is a perspective view of an electron beam flat display;
Figs. 10A and 10B show block diagrams Fig. 10A of an image signal input circuit of a liquid crystal display and a detailed diagram Fig. 10B of a display pixel unit and a sampling circuit;
Figs. 11A and 11B show examples in which an image signal is scanned on the display;
Fig. 12 is a timing chart for the 2-row simultaneous driving;
Figs. 13A to 13C show examples of signal polarities on the display;
Fig. 14 shows an image on the display when an NTSC signal including a white still image is interlace scanned at a high fidelity;
Figs. 15A and 15B show images Fig. 15A on the display when the NTSC signal including a white still image is 2-row simultaneous driven or is 2-row interpolation driven and also shows a voltage waveform Fig. 15B of each row; and
Figs. 16A and 16B show images Fig. 16A when the NTSC signal including the white still image is displayed on a display in which the number of rows of a display pixel section is only 1/2 of the number of scan lines and also shows a voltage waveform Fig. 16B of each row.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[Embodiment 1]

An embodiment 1 relates to an example in which the invention is applied to the 2-row interpolation driving of a TFT type liquid crystal display in which pixels are arranged in a delta shape. In the embodiment, two image input circuits are provided for one vertical data line. Fig. 3 shows a flow of signals in the embodiment 1. In Fig. 3, reference numeral 30-b denotes a sampling circuit and 40-b indicates a horizontal scanning circuit which construct a first image input circuit. Reference numeral 30-a denotes a sampling circuit; 40-a a horizontal scanning circuit; and 70 a temporary storage circuit. Those circuits construct a second image input circuit. Reference numeral 50 denotes a signal processing circuit which is divided to a system to directly lead a color signal to the sampling circuit 30-b and a system to lead the color signal to the sampling circuit 30-a through an inverting amplifier 80. The same component elements as those shown in Figs. 1A and 1B are designated by the same reference numerals and their descriptions are omitted here.

Fig. 4 shows further in detail the display pixel section 10, sampling circuit 30, and storage circuit 70 of the color liquid crystal display. The same color pixels (for example, B) of the display pixel section 10 are arranged so as to be deviated by 1.5 pixels for the adjacent rows in order to form a delta array. In the embodiment, since two image signals are inputted to one vertical data line, the storage circuit 70 (Fig. 3) is a circuit for storing the image signals for a period of time during which the first image input circuit is performing the writing operation. The storage circuit 70 is generally constructed by a capacitor 18. In this case, there is also a situation such that when the signal stored in the capacitor 18 is written to each pixel through the vertical data lines 14, a capacitive division occurs due to a parasitic capacitance of the vertical data lines 14 and a signal amplitude deteriorates.

In the embodiment, the apparatus further has: a reset transistor 17 to return the vertical data lines 14 to a reference potential (Vc); the switching transistors (sw1, sw2, ...) each for deciding a timing to write the image signals to the capacitor 18; and a transfer transistor 19 for transferring the signals of the capacitor 18 to each pixel through the vertical data lines 14.

Fig. 5 is a timing chart of the embodiment. When each pulse shown in the diagram is at the "H" level, the corresponding transistor is turned on. The reset transistor 17 is turned on by a pulse $\phi c$ for a T1 period and the vertical data lines 14 are reset to the reference potential Vc. Subsequently, at a T2 period, the color image 1H signal of odd1 is directly written to each pixel of the row g2 by a horizontal scan pulse $\phi H1$ (h11, h12, ... denote sampling periods of the pix-

els) and the vertical pulse $\phi g2$. At a T3 period, the vertical pulse $\phi g2$ is set to the "L" level, the TFT corresponding to the pixel of the relevant row is turned off, and the signal written in the corresponding pixel is held. At the same T2 period, a color 1H signal $V_T$ of oddl is written into the capacitor 18 in the storage circuit 70 by a horizontal scan pulse $\phi H2$ (h21, h22, ... denote sampling periods of the pixels). At a T3 period, the reset transistor 17 is made conductive by the pulse $\phi c$, and the residual charges of the vertical data lines 14 are eliminated, and the vertical data lines 14 are reset to the reference potential Vc. The transfer transistor 19 is made conductive by a pulse $\phi T$ at a T4 period, the TFTs corresponding to all of the pixels of the row g1 are turned on by the pulse $\phi g1$, and the color 1H signal $V_T$ of oddl stored in the capacitor 18 is written to each pixel of the row $g_1$. In this instance, since there is a fear such that the signal levels of the signals written to the row g1 drop due to the capacitive division or the like, it is preferable to provide an amplifier to the vertical data line 14. Deviations between the start timings of the pulses h21, h22, ... and the pulses h11, h12, ... corresponding to the pixels in the pulses $\phi H1$ and $\phi H2$ are set in consideration of the deviation of 1.5 pixels in the spatial arrangement of the same color signals between two rows.

The polarity of the image signal is inverted by the same pattern as that described in Fig. 13B. In the odd field, the signals of the same polarity are written to the adjacent two rows (rows g2 and g3; rows g4 and g5; ...) and the signal polarity is inverted every one horizontal scan (1H) (odd1, odd2, ...). In the even field, the signals of the opposite polarities are written to the adjacent two rows (rows g1 and g2; rows g3 and g4; ...) in which a combination is changed and the signal polarity is inverted every one horizontal scan (1H) (even1, even2, ...).

The embodiment has an n-frame inverting circuit for inverting the signal polarity every arbitrary n frames while performing the AC driving described above. Fig. 1B is the timing chart of the image signal when an attention is paid to a certain row (for example, row g2). It will be understood that although the image signal is inverted every field, the image signal is further inverted at a period of a large n-frame.

Fig. 6 is a signal processing block for performing the n-frame inversion of the embodiment. Reference numeral 50 denotes the signal processing circuit; 60 the control circuit; 80' an inverting amplifier; 51 an inverter; 52 a switch; and 53 a V counter. The signal processing circuit 50 executes a gamma process for converting image signals (R, G, B) to signals in consideration of the input/output characteristics of the liquid crystal. The signal processing circuit 50 forms the image signal that is inverted every 1H and one field by a pulse $\phi 1H/FLD$ of 1H which is outputted by the control circuit and instructs the 1-field inversion. The image signal outputted from the signal processing circuit is directly inputted to the sampling circuit 30-b and is inverted by the inverting amplifier 80' and the inverted signal is inputted to the sampling circuit 30-a. The inverting amplifier 80' executes the non-inverting amplification in the odd field and performs the inverting amplification in the even field by a field pulse $\phi FLD$. Thus, the display pixel section 10 is set to the signal polarities as shown in Fig. 13B. By always using the inverting amplifier 80' as an inverting amplifier, the display pixel section 10 can be set to the signal polarities as shown in Fig. 13C. As will be understood by paying an attention to a certain one row in Fig. 13C (for example, row g3), the signal polarities are also exchanged at 60 Hz in this case. When paying an attention to any adjacent two rows (for example, rows g3 and g4), since they have a pair of positive polarity and negative polarity, the luminance transition caused by AC driving is averaged and it is easy to see.

The case of directly inputting the pulse $\phi 1H/FLD$ and the case of inverting the pulse $\phi 1H/FLD$ through the inverter 51 are exchanged by using the switch 52 every n fields counted by the V counter 53. By the above exchanging operation, since the polarities of the image signals (R, G, B) are exchanged every 1H, one field, and n frames. Therefore, in the embodiment, the DC components as shown in the rows g3 and g6 in Fig. 15B are exchanged every n frames, the liquid crystal is not burned.

Although the embodiment has been shown and described with respect to the 1-system memory method, a 2-system memory method can be also used or a buffer circuit can be also provided at the post stage of the memory as shown in Fig. 7. Although the same color pixels have been connected to one data line in the embodiment, when pixels of various different colors are connected to one data line as shown in Fig. 8, it is sufficient to change scanning timings. In a monochromatic liquid crystal display device without any color filter, it is sufficient to perform the signal control for a monochromatic color. Although the above embodiment has been described with respect to the example in which the n-frame inversion is further executed in the 1H/1 field inverting system, the invention can be also similarly applied to an inverting system as shown in Fig. 1B so long as it executes the field deviation driving such that a plurality of rows to be combined are changed every field.

In the embodiment, a display to write the color signals which are outputted from the signal processing circuit 50 to two rows at different timings in a series of one horizontal scan (1H) periods as shown at T1 to T4 in Fig. 5. Therefore, as compared with the two-row simultaneous driving method, the number of sampling times of the image signal is doubled, so that the resolution is improved and a moire due to an aliasing distortion of the sampling can be also reduced. Since the signal polarities are inverted as shown in

Fig. 13B, when an attention is paid to one row, the inversion signal is written every field (60 Hz), so that a flickering which is conspicuous for the human eyes doesn't occur.

[Embodiment 2]

The embodiment 2 relates to an example in which the invention is applied to the 2-row simultaneous driving of an STN type liquid crystal display of a simple matrix wiring in which pixels are arranged in lines. In the embodiment 2, one image input circuit is provided for one data line. Fig. 1A shows a signal processing block diagram for performing the n-frame inversion of the embodiment. A display section 1 includes the display pixel section, horizontal scanning circuit, vertical scanning circuit, and the like. The control circuit 60 generates a pulse $\phi$FRP to invert the signals every 1H and one field, thereby inverting the image signals (R, G, B) every 1H and one field. The case of inputting the pulse $\phi$FRP without inverting and the case of inverting the pulse $\phi$FRP through the inverter 51 and inputting are exchanged by using the switch 52 every n fields counted by the counter 53. By the above operation, the polarities of the image signals (R, G, B) are exchanged every 1H and one field and n frames. For example, they are inverted every 30 frames as n frames. For this purpose, the counter 53 counts 60 fields and alternately exchanges a pulse $\phi$V which is generated from the control circuit to the in-phase and opposite phase of $\phi$FRP every 60 fields (one minute).

In the embodiment as well, since the DC components as shown in the rows g3 and g6 in Fig. 15B are exchanged every n frames, the liquid crystal is not burned. In the embodiment, since the same image signal is inputted to the pixels locating at the same column in two rows, a simple matrix wiring of a simple structure can be used without using any switching element or the like. Therefore, the whole manufacturing costs are cheap. Although the embodiment has been described with respect to the STN type liquid crystal display of the simple matrix wiring in which the pixels are arranged in lines, any one of the displays which can perform the 2-row simultaneous driving can be used in the embodiment. For example, the liquid crystal material is not limited to the super twisted nematic liquid crystal (STN) but can also use a twisted nematic liquid crystal (TN) or a ferroelectric liquid crystal (FLC). The wiring is not limited to only the simple matrix wiring but can also use an active matrix wiring using a switching element of two or three terminals.

[Embodiment 3]

The embodiment 3 relates to a display example of a panel in which the number of rows of a display pixel section is only 1/2 of the number of scan lines of the image signal. In a manner similar to the embodiment 2, only one image input circuit is provided for one data line. A TFT type LCD is used as a display. When the image signals are inputted to the display pixel section, although the vertical scanning circuit has sequentially selected every two rows in the embodiment 2, the vertical scanning circuit sequentially selects only every row in the embodiment 3. Since the switching transistor is provided for each pixel in the embodiment 3, the pulse that is outputted from the vertical scanning circuit is the pulse to turn on the switching transistor. The other driving method is substantially the same as that of the embodiment 2. The image signals are inverted every 1H and one field and n frames by using the circuit as described in Fig. 1A.

According to the embodiment 3, since the DC component as shown in the row g6 in Fig. 16B is exchanged every n frames, the liquid crystal is not burned. Although the embodiment 3 has been described with respect to the case of using the TFT type LCD as a display, any other LCD of the MIM type or simple matrix type can be also used.

[Embodiment 4]

The embodiment 4 relates to an example in which the invention is applied to the electron beam flat display. As a display, a flat panel in which each pixel has an electron source and which has a fluorescent plate for exciting and emitting the light by electrons which are emitted from the electron sources is used. Fig. 9 simply shows such an electron beam flat display. In the diagram, reference numeral 105 denotes a rear plate; 106 a barrier; and 107 a phase plate. An airtight vessel is constructed by those component elements and the inside of the display is maintained at a vacuum state. Reference numeral 101 denotes a substrate; 102 an electron source; 103 a row direction wiring; and 104 a column direction wiring. Those component elements are fixed to the rear plate 105. Reference numeral 108 denotes a fluorescent material and 109 indicates a metal back which are fixed to the phase plate 107. By colliding electrons to the fluorescent material 108, the electron source 102 excites the fluorescent material 108 and emits the light. As a fluorescent material, a material which emits three primary colors of red, blue, and green is arranged. The metal back 109 has roles for improving a light using efficiency by mirror reflecting the light emitted from the fluorescent material 108, for protecting the fluorescent material 108 from the collision of the electrons, and for accelerating the electrons by being applied with a high voltage from a high voltage input terminal Hv. There are (M x N) electron sources 102 as a whole (M electron sources in the vertical direction and N electron sources in the horizontal direction). Those electron sources are connected by the M row

direction wirings 103 and the N column direction wirings 104 which perpendicularly cross each other. Dx1, Dx2, ..., DxM denote input terminals of the row direction wirings. Dy1, Dy2, ..., DyN denote input terminals of the column direction wirings. The row direction wirings 103 become data wirings. The column direction wirings 104 become scan wirings.

Even in such an electron beam flat display, the 2-row simultaneous driving as shown in the embodiment 2 or the driving as shown in the embodiment 3 in which the number of rows is equal to only 1/2 of the number of scan lines of one frame of the image signal can be executed. By exchanging the case where the pulse $\phi$FRP is inputted and the case where the pulse $\phi$FRP is inverted through the inverter 51 by using the switch 52 every n fields counted by the counter 53 as described in Fig. 1A of the embodiment 2, the polarities of the image signals are exchanged every 1H and one field and n fields. Therefore, even when a still image is inputted, the device is not deteriorated.

## Claims

1. A display wherein an image signal can be inputted to a same row at an odd field period and an even field period,
   characterized by means for inverting a polarity of said image signal every field and for, further, inverting said polarity at arbitrary frames.

2. A display according to claim 1, characterized in that an image signal of one horizontal scan is inputted to a plurality of rows and a combination of said rows is changed for the odd field period and the even field period.

3. A display according to claim 2, characterized in that said plurality of rows are two rows.

4. A display according to claim 2, characterized in that pixels are arranged in a delta shape and a sampling period of the image signal which is inputted to said plurality of rows is set in accordance with said delta-shaped arrangement.

5. A display according to claim 2, characterized in that pixels are arranged in lines and a sampling period of the image signal which is inputted to said plurality of rows is set in accordance with said line arrangement.

6. A display according to claim 1, characterized in that the image signal of one horizontal scan is inputted to the same row for the odd field period and the even field period.

7. A display according to claim 6, characterized in that said row is one row.

8. A display according to any one of claims 1 to 7, characterized in that said means for inverting the polarity every said arbitrary frames inverts said polarity every period of time from 0.13 second (7.5 Hz) to 60 minutes.

9. A display according to any one of claims 1 to 7, characterized in that said means for inverting the polarity every said arbitrary frames inverts said polarity at a period of time from one second (1 Hz) to one minute.

10. A liquid crystal display according to any one of claims 1 to 9, characterized by having a pair of substrates and a liquid crystal material sandwiched between said substrates.

11. An active matrix liquid crystal display according to claim 10, characterized in that a switching element is arranged every pixel on one of said pair of substrates.

12. An active matrix liquid crystal display according to claim 11, characterized in that said switching element is a TFT.

13. An electron beam flat display according to any one of claims 1 to 9, characterized by further having a fluorescent material and an electron source every pixel.

14. A method of driving a display wherein an image signal is inputted to a same row at an odd field period and an even field period,
   characterized in that a polarity of said image signal is inverted every field and said polarity is further inverted at arbitrary frames.

15. A method according to claim 14, characterized in that an image signal of one horizontal scan is inputted to a plurality of rows and a combination of said rows is changed for the odd field period and the even field period.

16. A method according to claim 15, characterized in that said plurality of rows are two rows.

17. A method according to claim 15 or 16, characterized in that pixels are arranged in a delta shape and a sampling period of the image signal which is inputted to said plurality of rows is set in accordance with said delta-shaped arrangement.

18. A method according to claim 15 or 16, characterized in that pixels are arranged in lines and a sampling period of the image signal which is inputted

to said plurality of rows is set in accordance with said line arrangement.

19. A method according to claim 14, characterized in that the image signal of one horizontal scan is inputted to the same row for the odd field period and the even field period.

20. A method according to claim 19, characterized in that said row is one row.

21. A method according to any one of claims 14 to 20, characterized in that said means for inverting the polarity every said arbitrary frames inverts said polarity every period of time from 0.13 second (7.5 Hz) to 60 minutes.

22. A method according to any one of claims 14 to 20, characterized in that said means for inverting the polarity every said arbitrary frames inverts said polarity at a period of time from one second (1 Hz) to one minute.

23. A method according to any one of claims 14 to 22, characterized in that said display has a pair of substrates and a liquid crystal material sandwiched between said substrates, thereby constructing a liquid crystal display.

24. A method according to claim 23, characterized in that a switching element is arranged every pixel on one of said pair of substrates, thereby constructing an active matrix liquid crystal display.

25. A method according to claim 24, characterized in that said switching element is a TFT.

26. A method according to any one of claims 14 to 22, characterized in that said display has a fluorescent material and an electron source every pixel, thereby constructing an electron beam flat display.

FIG. 1A

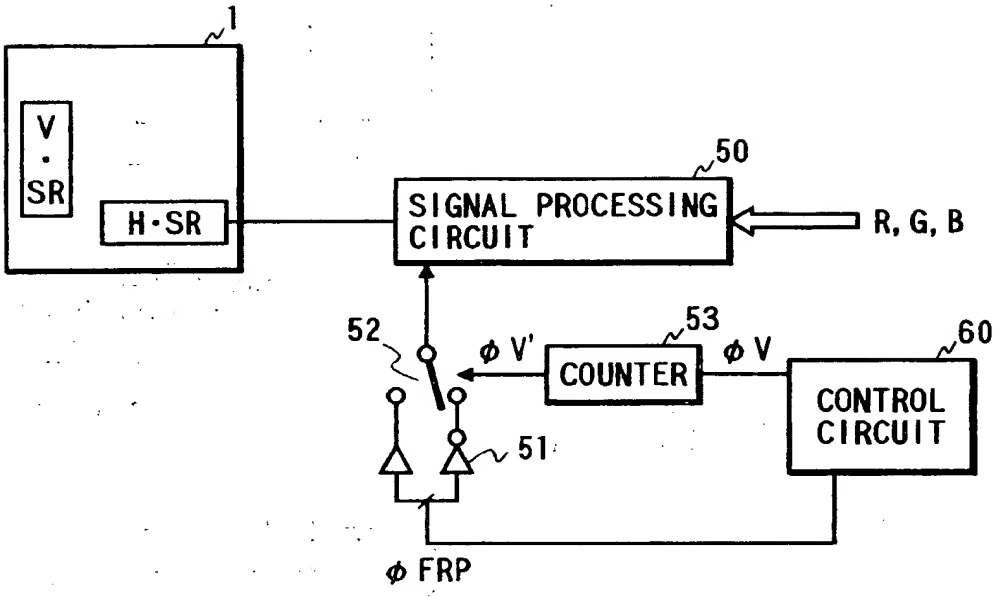



FIG. 1B

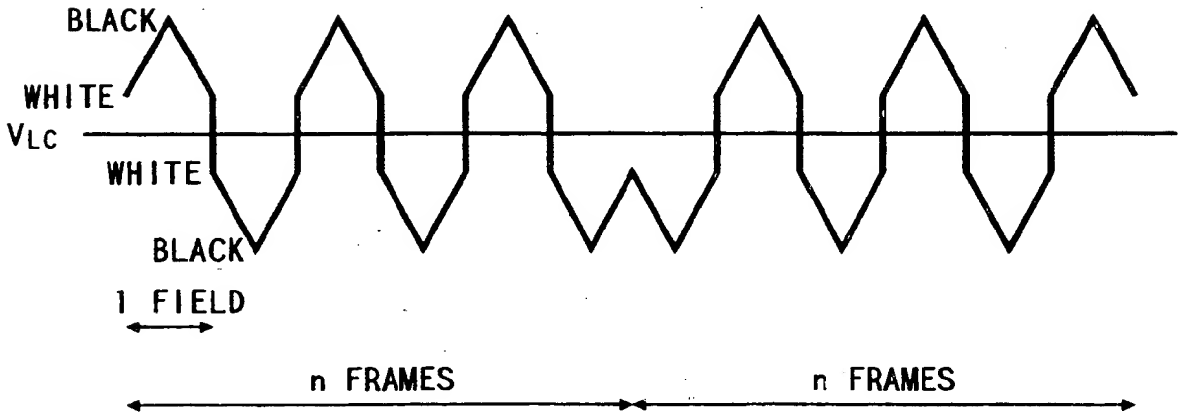


FIG. 2A

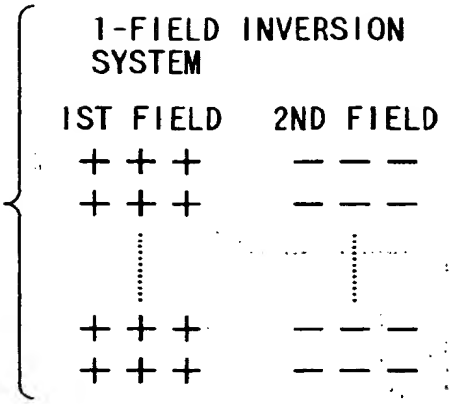



FIG. 2B

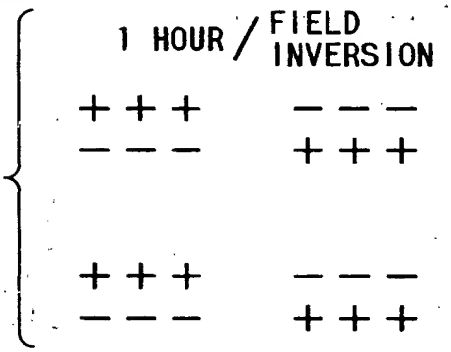



FIG. 2C

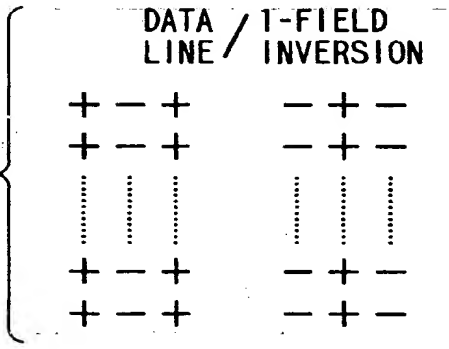



FIG. 2D

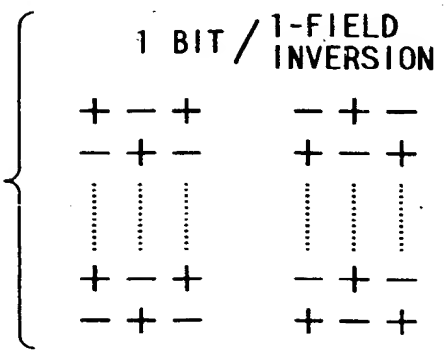


FIG. 3

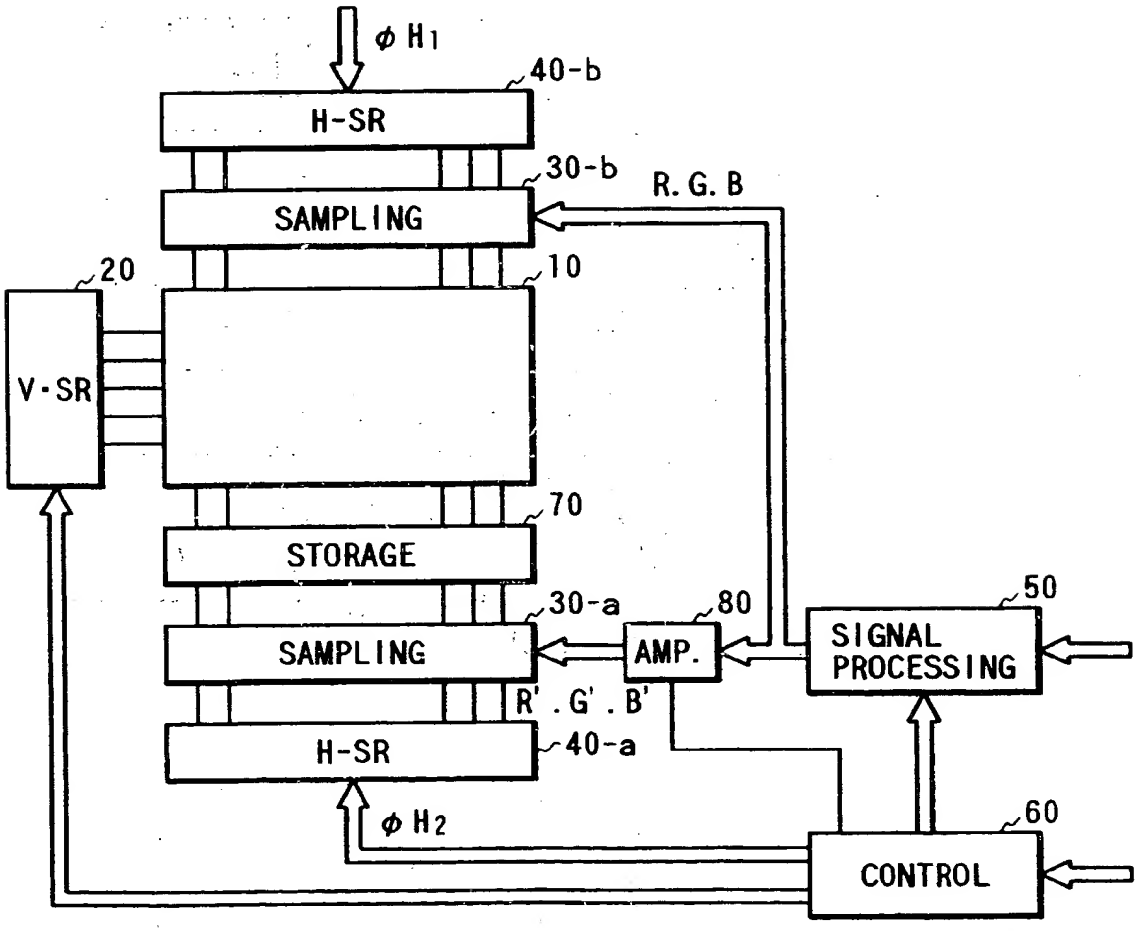
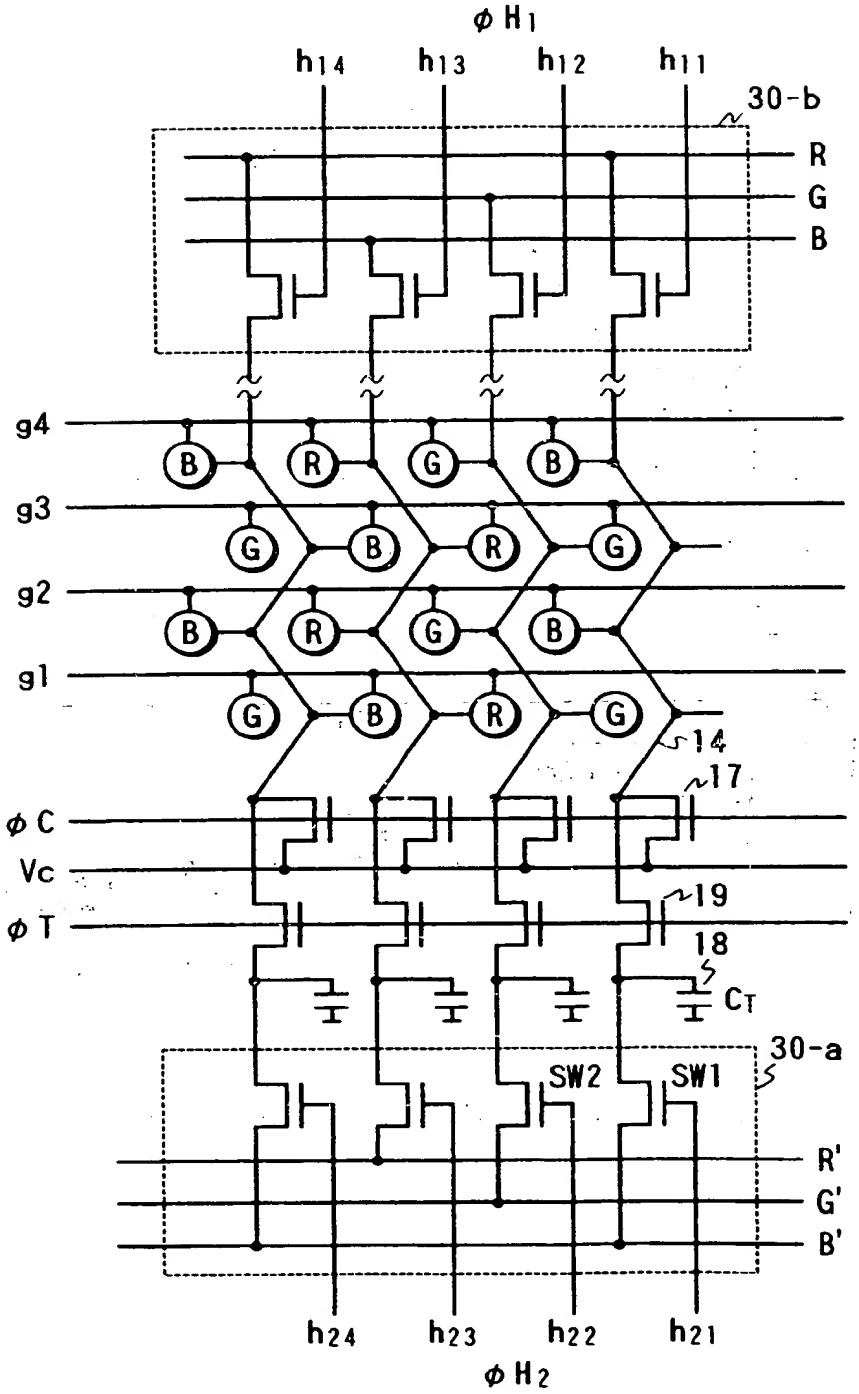


FIG. 4



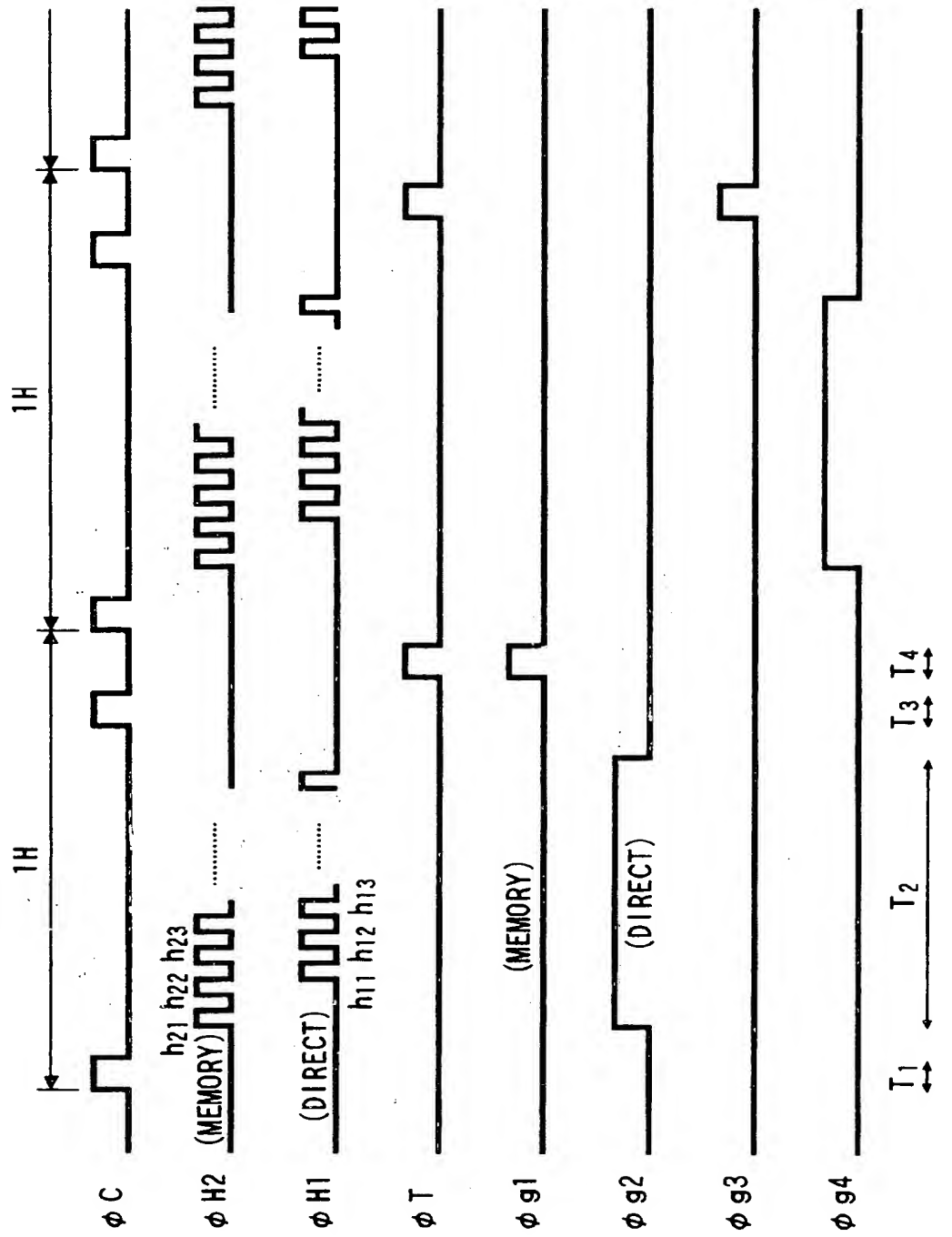



FIG. 5

FIG. 6

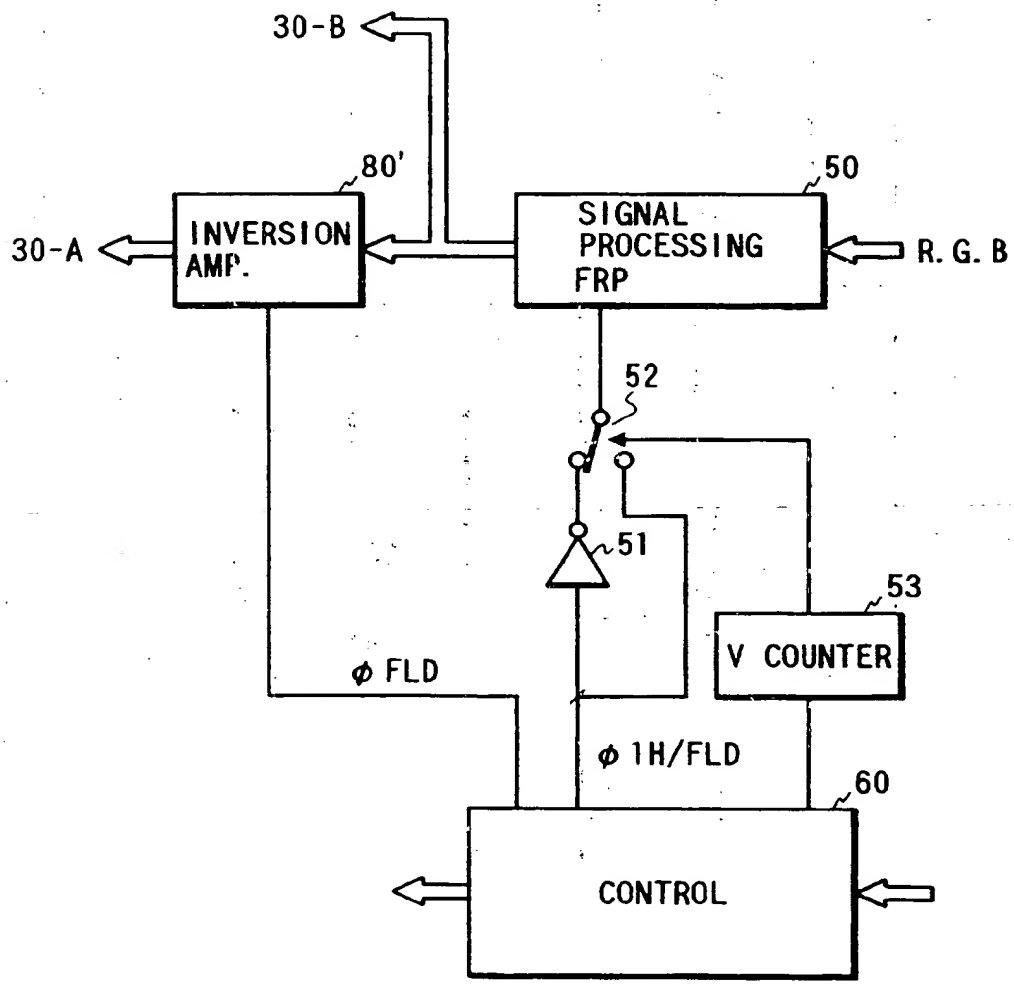


FIG. 7

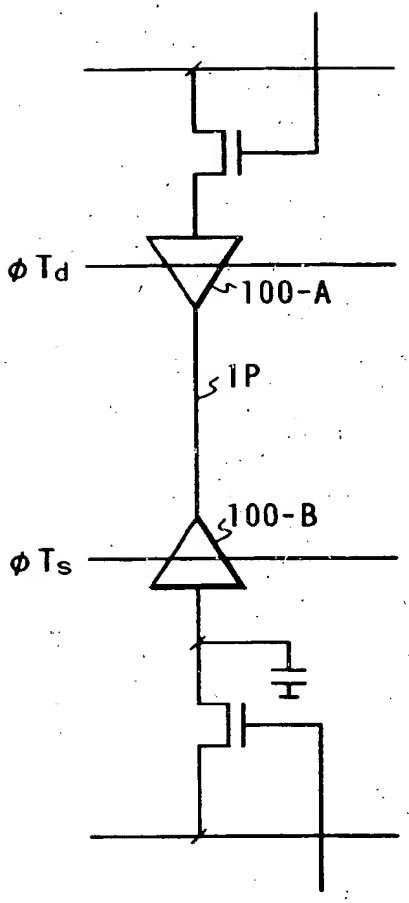



FIG. 8

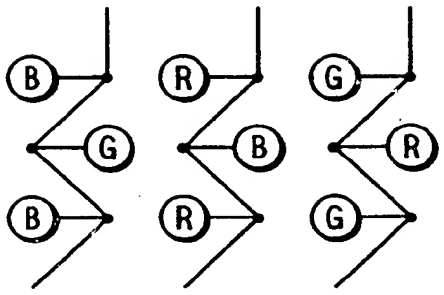


FIG. 9

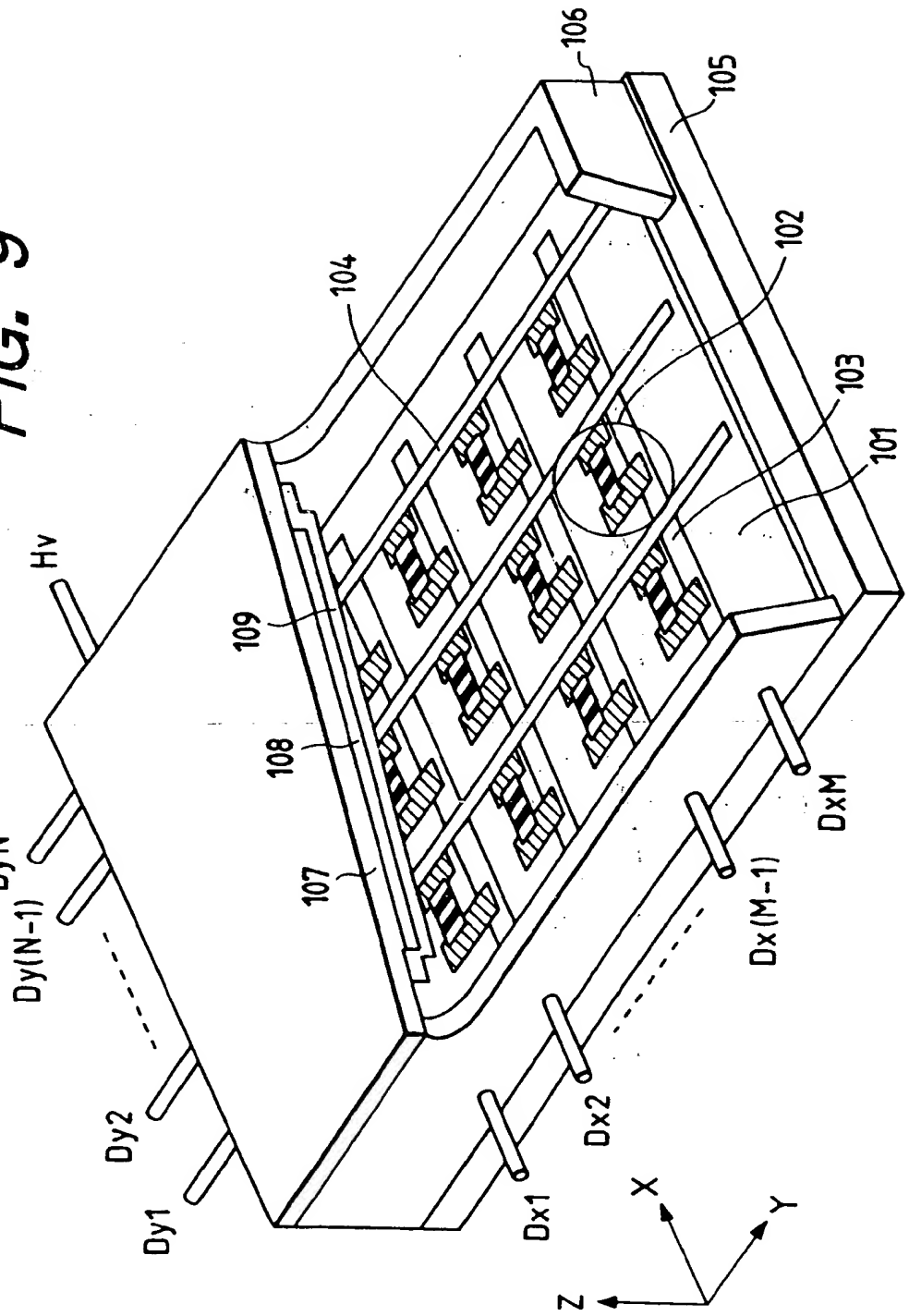


FIG. 10A

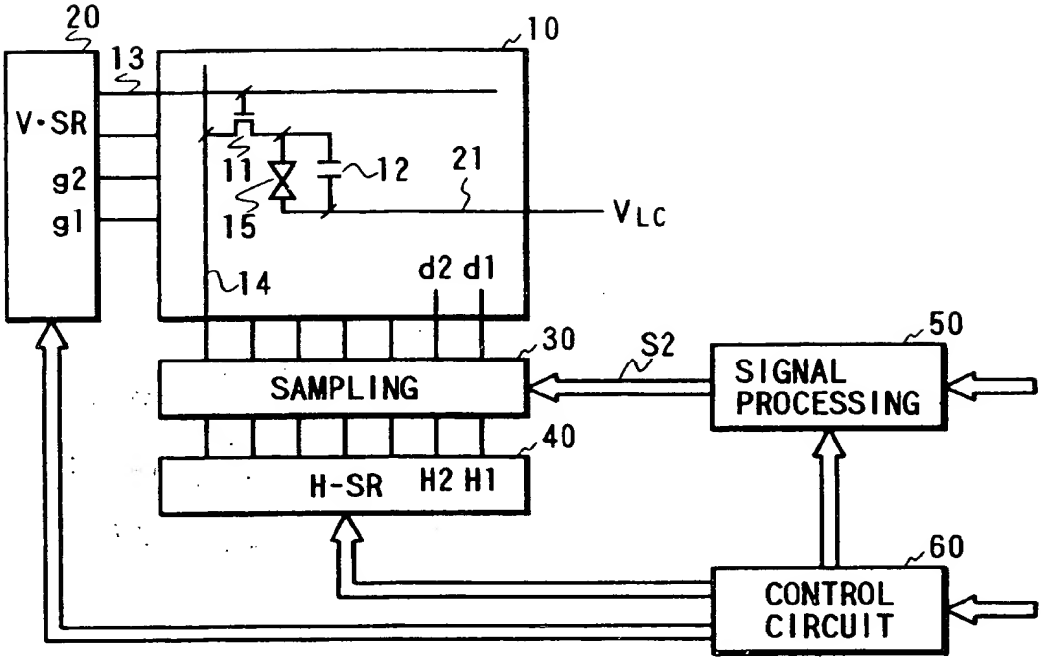



FIG. 10B

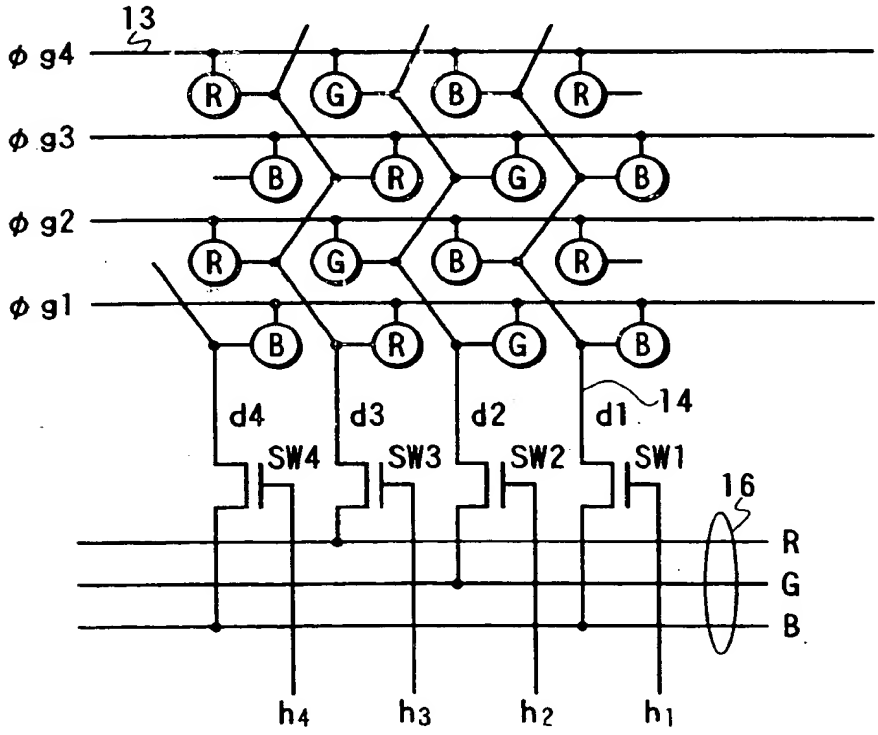


FIG. 11A

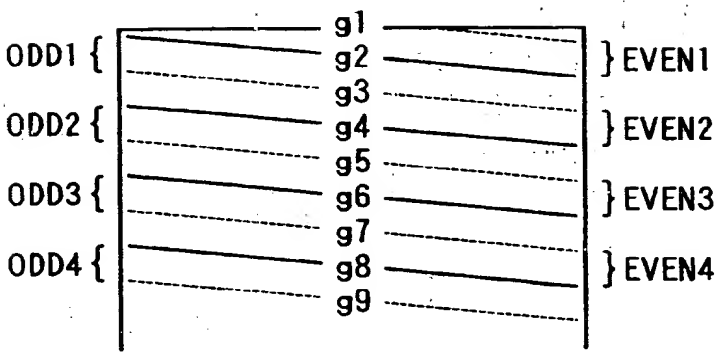
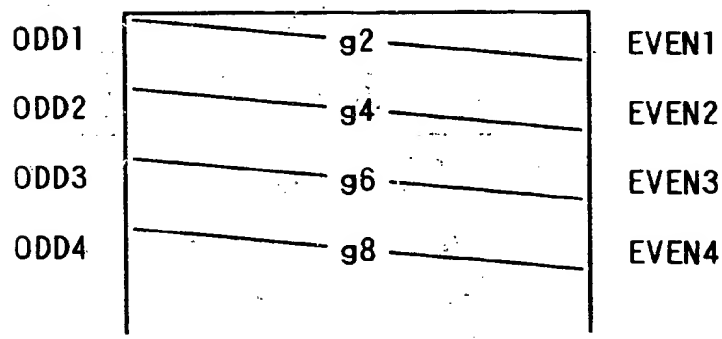



FIG. 11B



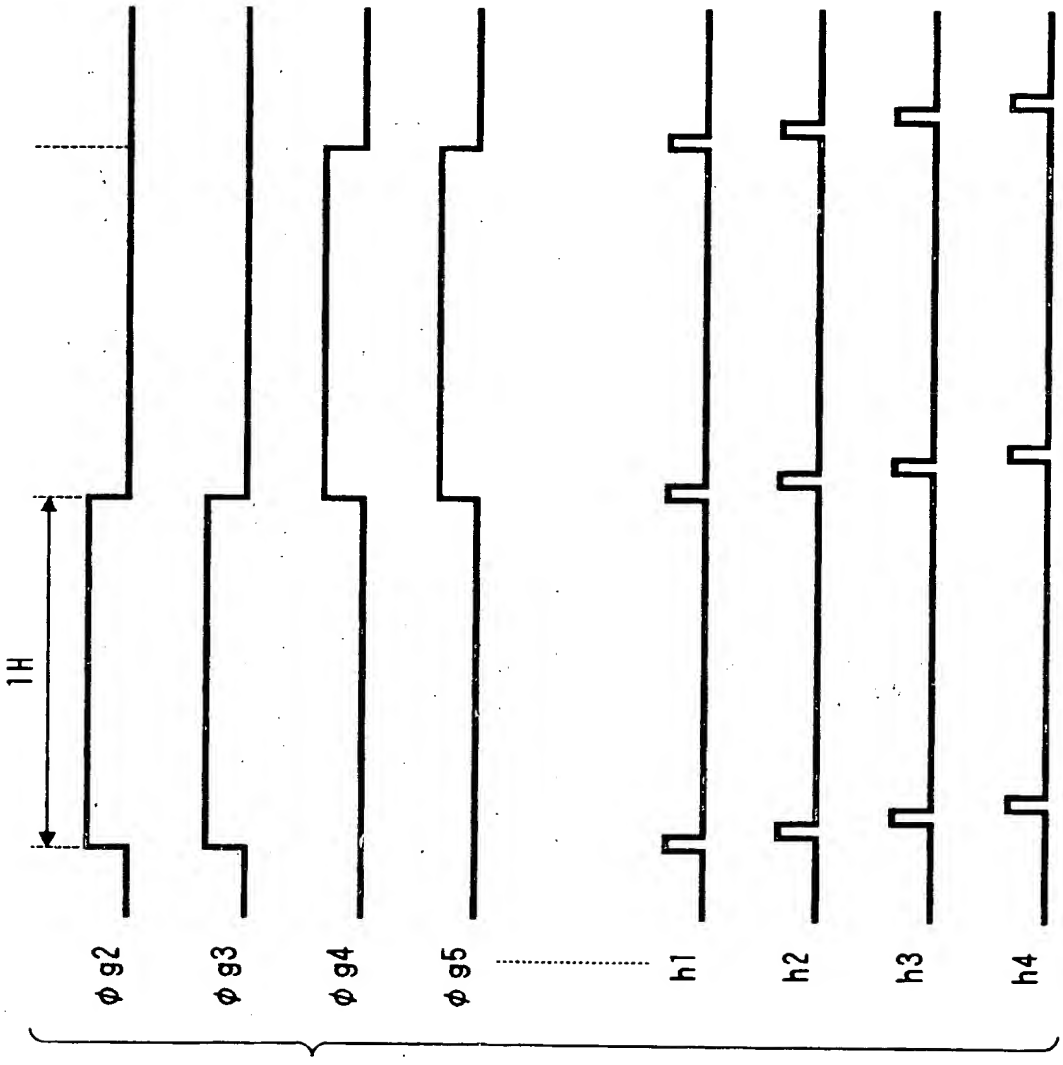



FIG. 12

FIG. 13A

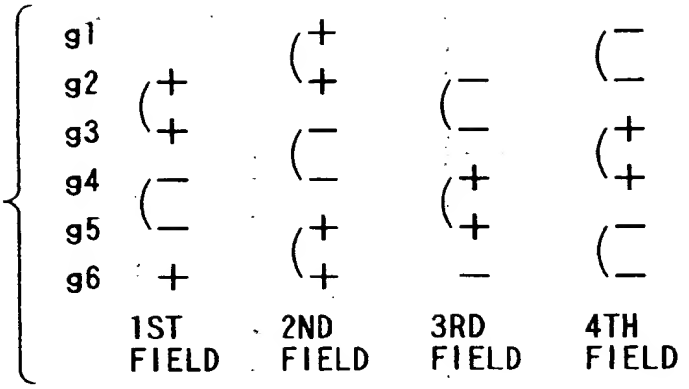



FIG. 13B

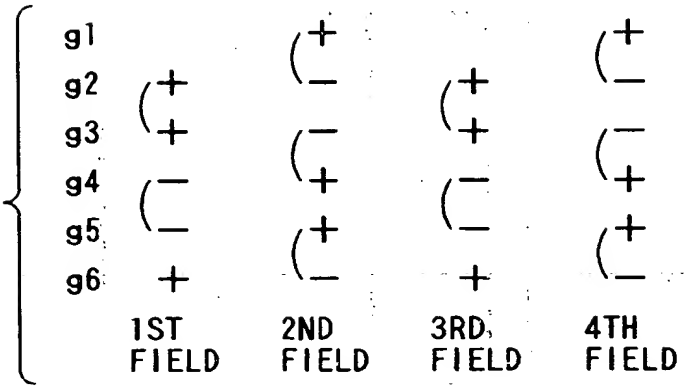



FIG. 13C

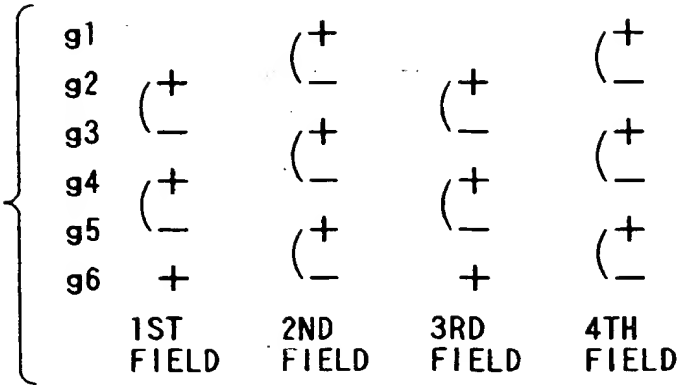


FIG. 14

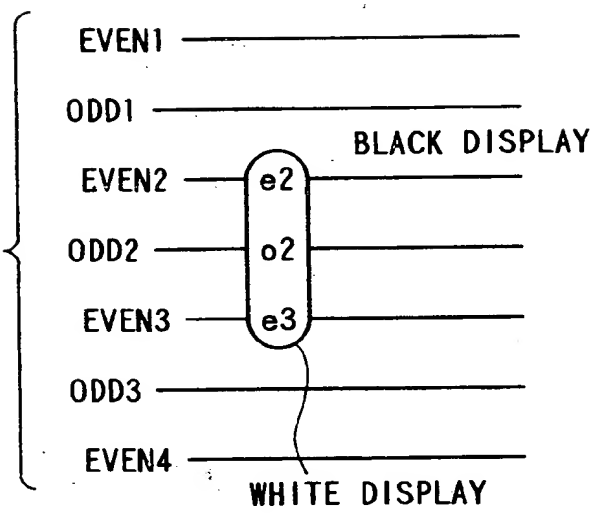


FIG. 15A

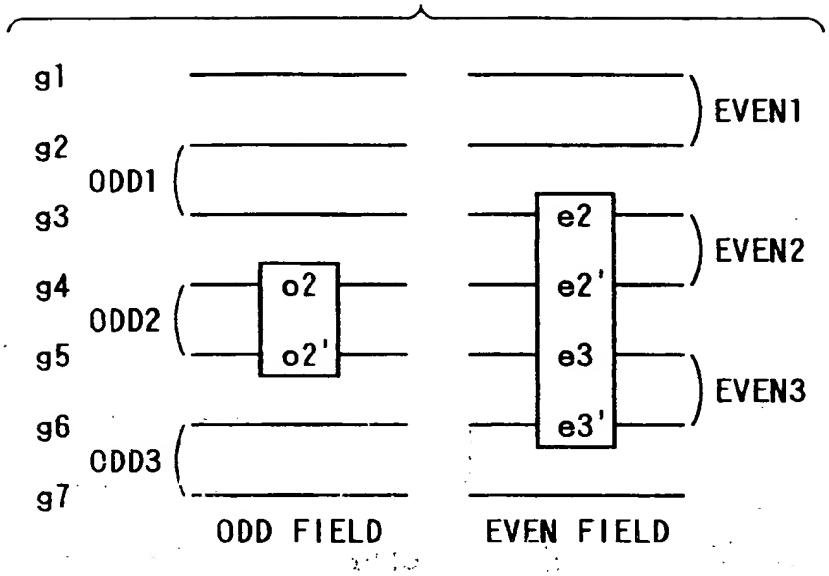



FIG. 15B

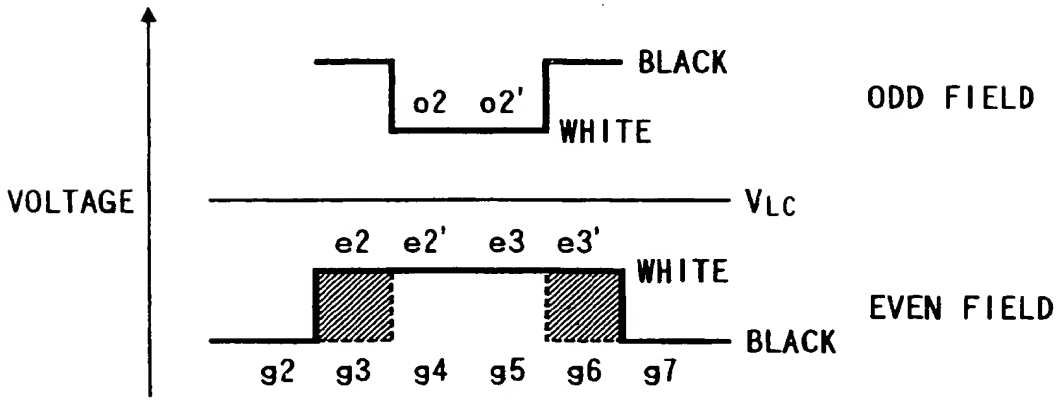


FIG. 16A

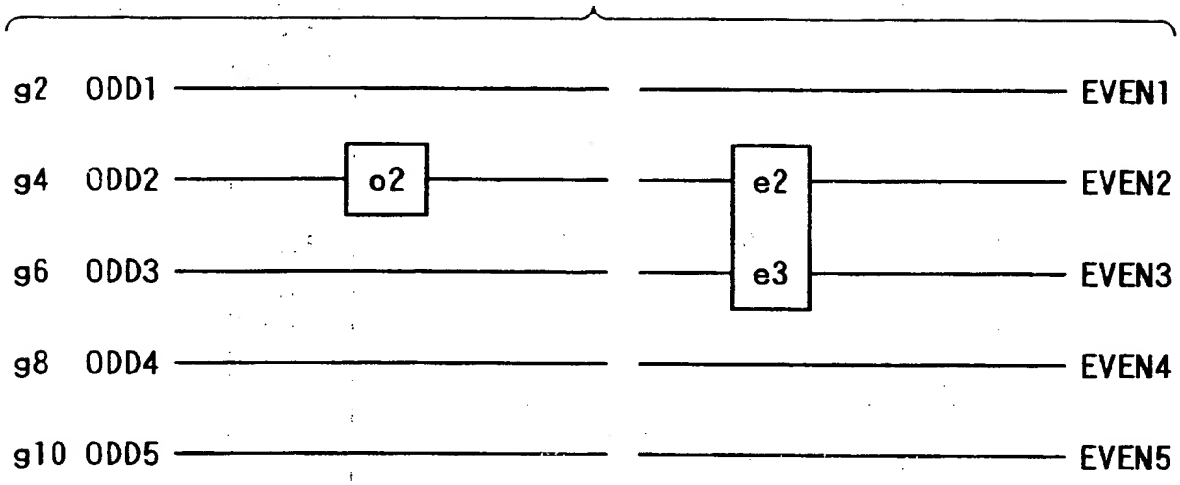
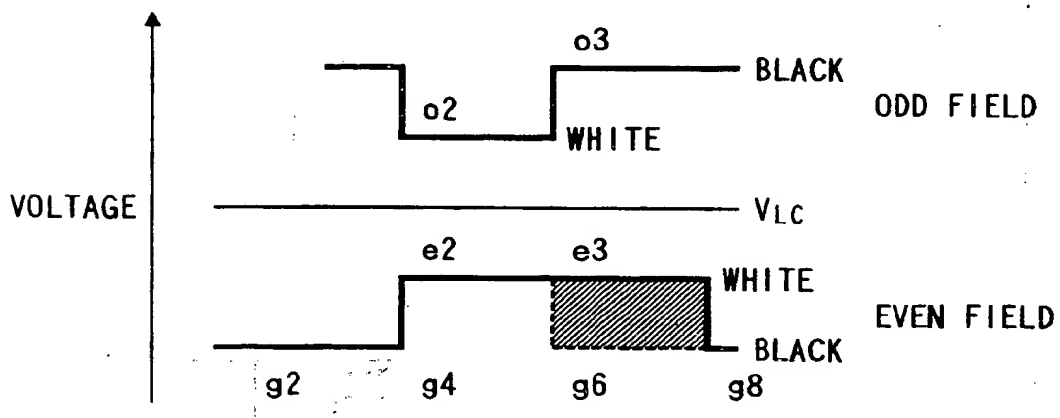



FIG. 16B



European Patent Office

# EUROPEAN SEARCH REPORT

Application Number
EP 95 30 3712

## DOCUMENTS CONSIDERED TO BE RELEVANT

| Category | Citation of document with indication, where appropriate, of relevant passages | Relevant to claim | CLASSIFICATION OF THE APPLICATION (Int.Cl.6) |
|---|---|---|---|
| Y | EP-A-0 371 665 (SHARP K.K.)<br>* column 1, line 34 - line 45 *<br>* column 10, line 30 - column 14, line 32 *<br>* figures 1-7 * | 1-3,6, 10-12, 14-16, 19,23-25 | G09G3/36 |
| Y | EP-A-0 416 550 (HITACHI LTD.)<br>* column 1, line 51 - column 3, line 33 *<br>* column 7, line 27 - line 36 *<br>* column 8, line 29 - line 55 *<br>* column 9, line 12 - line 17 *<br>* column 27, line 16 - line 22 *<br>* figures 1-3,28 * | 1-3,6, 10-12, 14-16, 19,23-25 | |
| A | EP-A-0 368 572 (SHARP K.K.)<br>* column 28, line 14 - column 29, line 54 *<br>* figures 12-14 * | 14,17 | TECHNICAL FIELDS SEARCHED (Int.Cl.6)<br>G09G |
| A | EP-A-0 486 284 (SEL SEMICONDUCTOR ENERGY LABORATORY CO. LTD.)<br>* column 18, line 1 - line 8 *<br>* claims 12,13 * | 1,14 | |

The present search report has been drawn up for all claims

| Place of search | Date of completion of the search | Examiner |
|---|---|---|
| THE HAGUE | 4 October 1995 | Farricella, L |

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
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P : intermediate document

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E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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